In the Abstract, please substitute the following:

Abstract

A method, apparatus, and system for controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across these capacitors will not exceed the breakdown voltage limitation of these capacitors. The voltage level between the first and second nodes of the integrated circuit can vary from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, respectively. A first capacitor and a second capacitor are connected in series between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors. The voltage level of the middle node is set to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does not exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor.

Claims

The proposed amendments are set forth below, which includes amendments to claims 1, 10 and 15.

1. (Currently Amended) A method of controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across [these] the capacitors [will] do not exceed the breakdown voltage limitation of these capacitors, the voltage level between the first and second nodes varying from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, the first power state corresponds to a low power state and the second power state corresponds to a high power state, the method comprising:

connecting in series a first capacitor and a second capacitor between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors; and

setting the voltage level of the middle node to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does not exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor.

2. The method of claim 1 wherein setting the voltage level of the middle node comprises: